What is claimed is :

SUB B1

1. A semiconductor device comprising :

an interconnection board ; and

a high rigidity plate securely fixed to said interconnection board, said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent.

2. The semiconductor device as claimed in claim 1, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

3. The semiconductor device as claimed in claim 1, wherein said high rigidity plate is made of a metal.

4. The semiconductor device as claimed in claim 1, wherein said high rigidity plate is made of an alloy.

5. The semiconductor device as claimed in claim 1, wherein said high rigidity plate is made of a ceramic.

6. The semiconductor device as claimed in claim 1, wherein a base material of said interconnection board is an organic insulative material.

7. The semiconductor device as claimed in claim 6, wherein said organic material is a polymer resin material.

8. A semiconductor device comprising :

an interconnection board having first and second surfaces ;

at least a semiconductor chip mounted on said first surface of said interconnection board ; and

a high rigidity plate securely fixed to said second surface of said interconnection board, said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent.

SUB B2

9. The semiconductor device as claimed in claim 8, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

10. The semiconductor device as claimed in claim 8, wherein said high rigidity plate is made of a metal.

11. The semiconductor device as claimed in claim 8, wherein said high rigidity plate is made of an alloy.

12. The semiconductor device as claimed in claim 8, wherein said high rigidity plate is made of a ceramic.

13. The semiconductor device as claimed in claim 8, wherein a base material of said interconnection board is an organic material.

14. The semiconductor device as claimed in claim 13, wherein said organic material is a polymer resin material.

15. The semiconductor device as claimed in claim 8, wherein said at least semiconductor chip is bonded via bumps to said second surface of said interconnection board.

16. The semiconductor device as claimed in claim 15, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

17. The semiconductor device as claimed in claim 16, further comprising at least a heat spreader provided on said at least semiconductor chip.

SUB B3

18. A semiconductor device comprising :

an interconnection board having first and second surfaces ;

at least a semiconductor chip mounted on said first surface of said interconnection board ; and

a buffer layer having a first surface in contact with said second surface of said interconnection board and also said buffer layer having a second surface on which at least an external electrode is provided, and said buffer layer having at least an electrical contact between said interconnection board and said at least external electrode, and said buffer layer being capable of absorbing and/or relaxing a stress applied to said at least external electrode to make said interconnection board free from application of said stress.

19. The semiconductor device as claimed in claim 18, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

20. The semiconductor device as claimed in claim 18, wherein said at least external electrode comprises plural external electrodes.

21. The semiconductor device as claimed in claim 18, wherein said external electrode comprises a solder ball.

22. The semiconductor device as claimed in claim 18, wherein said external electrode comprises a pin electrode.

23. The semiconductor device as claimed in claim 18, wherein said external electrode comprises a coil-spring electrode.

24. The semiconductor device as claimed in claim 18, wherein said external electrode comprises a generally column shaped electrode.

25. The semiconductor device as claimed in claim 24, wherein said generally column shaped electrode comprises a straight column shaped electrode which is uniform in horizontal cross sectional area from a bottom to a top thereof.

26. The semiconductor device as claimed in claim 24, wherein said generally column shaped electrode comprises a center-pinched column shaped electrode which decreases in horizontal cross sectional area toward an intermediate level thereof.

27. The semiconductor device as claimed in claim 18, wherein said buffer layer comprises :

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode.

28. The semiconductor device as claimed in claim 27, wherein said plural generally column shaped electrically conductive layers are made of a metal.

29. The semiconductor device as claimed in claim 18, wherein said buffer layer comprises :

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode ; and

an stress absorption layer filling gaps between said plural generally column shaped electrically conductive layers, and said stress absorption layer being lower in rigidity than said plural generally column shaped electrically conductive layers, and said stress absorption layer surrounding said plural generally column shaped electrically conductive layers so that said stress absorption layer is in tightly contact with said plural generally column shaped electrically conductive layers.

30. The semiconductor device as claimed in claim 29, wherein said plural generally column shaped electrically conductive layers are made of a metal.

31. The semiconductor device as claimed in claim 29, wherein said stress absorption layer is made of an organic insulative material.

32. The semiconductor device as claimed in claim 18, wherein said buffer layer comprises :

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode ;

a supporting plate having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board ; and

a supporting sealing resin material filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

33. The semiconductor device as claimed in claim 32, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

34. The semiconductor device as claimed in claim 32, wherein said

plural generally column shaped electrically conductive layers are made of a metal.

35. The semiconductor device as claimed in claim 32, wherein said supporting sealing resin material is made of an organic insulative material.

36. The semiconductor device as claimed in claim 18, further comprising a supporting layer on said second surface of said buffer layer for supporting said external electrode.

37. The semiconductor device as claimed in claim 35, wherein said supporting layer further comprises :

a supporting plate having plural holes, into which said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer to form an inter-space between said supporting plate and said second surface of said buffer layer ; and

a supporting sealing resin material filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said parts of said external electrodes for supporting said external electrodes.

38. The semiconductor device as claimed in claim 18, wherein said at least semiconductor chip is bonded via bumps to said second surface of said interconnection board.

39. The semiconductor device as claimed in claim 38, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

40. The semiconductor device as claimed in claim 39, further comprising at least a heat spreader provided on said at least semiconductor chip.

41. The semiconductor device as claimed in claim 38, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

42. The semiconductor device as claimed in claim 41, further comprising :

a stiffener extending on a peripheral region of said buffer layer ; and

at least a heat spreader provided on said at least semiconductor chip and on said stiffener.

SUB B5

43. A semiconductor device comprising :

an interconnection board having first and second surfaces ;

at least a semiconductor chip mounted on said first surface of said interconnection board ;

external electrodes fixed to external electrode pads on said second surface of said interconnection board ; and

a supporting layer on said second surface of said interconnection board for supporting said external electrodes.

SUB B5 Cont.

44. The semiconductor device as claimed in claim 43, wherein said supporting layer further comprises :

a supporting plate having plural holes, into which said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer to form an inter-space between said supporting plate and said second surface of said buffer layer ; and

a supporting sealing resin material filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said parts of said external electrodes for supporting said external electrodes.

45. The semiconductor device as claimed in claim 43, wherein said at least semiconductor chip is bonded via bumps to said second surface of said interconnection board.

46. The semiconductor device as claimed in claim 45, wherein further comprising a sealing resin material provided on said first surface of

said interconnection board for sealing said at least semiconductor chip and said bumps.

47. The semiconductor device as claimed in claim 46, further comprising at least a heat spreader provided on said at least semiconductor chip.

48. The semiconductor device as claimed in claim 45, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

SUB B6

49. The semiconductor device as claimed in claim 48, further comprising :

a stiffener extending on a peripheral region of said buffer layer ; and

at least a heat spreader provided on said at least semiconductor chip and on said stiffener.

50. The semiconductor device as claimed in claim 43, wherein said external electrodes connected through plural generally column shaped electrically conductive layers to external electrode pads on said second surface of said interconnection board, and said supporting layer further comprises :

a supporting plate having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board ; and

a supporting sealing resin material filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

51. The semiconductor device as claimed in claim 50, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

52. The semiconductor device as claimed in claim 50, wherein said plural generally column shaped electrically conductive layers are made of a metal.

53. The semiconductor device as claimed in claim 50, wherein said

supporting sealing resin material is made of an organic insulative material.

54. The semiconductor device as claimed in claim 43, wherein said external electrode comprises a solder ball.

55. The semiconductor device as claimed in claim 43, wherein said external electrode comprises a pin electrode.

56. The semiconductor device as claimed in claim 43, wherein said external electrode comprises a coil-spring electrode.

57. The semiconductor device as claimed in claim 18, wherein said external electrode comprises a generally column shaped electrode.

58. The semiconductor device as claimed in claim 24, wherein said generally column shaped electrode comprises a straight column shaped electrode which is uniform in horizontal cross sectional area from a bottom to a top thereof.

59. The semiconductor device as claimed in claim 24, wherein said generally column shaped electrode comprises a center-pinched column shaped electrode which decreases in horizontal cross sectional area toward an intermediate level thereof.

60. A method of forming an interconnection board, wherein during formation of said interconnection board, said interconnection board remains securely fixed to a high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent.

61. The method as claimed in claim 60, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

62. The method as claimed in claim 60, further comprising the step of : completely removing said high rigidity plate from said interconnection board, after said interconnection board is fabricated on said high rigidity plate.

63. The method as claimed in claim 62, wherein said high rigidity plate is made of a metal.

64. The method as claimed in claim 62, wherein said high rigidity plate is made of an alloy.

65. The method as claimed in claim 62, wherein said high rigidity plate is made of a ceramic.

66. The method as claimed in claim 62, wherein a base material of said interconnection board is an organic insulative material.

67. The method as claimed in claim 66, wherein said organic material is a polymer resin material.

68. The method as claimed in claim 60, further comprising the step of : selectively removing said high rigidity plate from said interconnection board to form plural generally column shaped electrically conductive layers on said interconnection board, after said interconnection board is fabricated on said high rigidity plate.

69. The method as claimed in claim 68, further comprising the step of : forming external electrodes on said plural generally column shaped electrically conductive layers so that said external electrodes are electrically connected through said plural generally column shaped electrically conductive layers to said interconnection board.

70. The method as claimed in claim 68, further comprising the step of : forming an stress absorption layer being lower in rigidity than said plural generally column shaped electrically conductive layers, which fills gaps between said plural generally column shaped electrically conductive layers, so that said stress absorption layer surrounds said plural generally column shaped electrically conductive layers, whereby said stress

absorption layer is in tightly contact with said plural generally column shaped electrically conductive layers.

71. The method as claimed in claim 70, further comprising the step of : forming external electrodes on said plural generally column shaped electrically conductive layers so that said external electrodes are electrically connected through said plural generally column shaped electrically conductive layers to said interconnection board.

72. The method as claimed in claim 71, further comprising the step of :

forming a supporting plate having plural holes, into which said external electrodes are inserted, so that said supporting plate extends in parallel to said second surface of said buffer layer to form an inter-space between said supporting plate and said second surface of said buffer layer ; and

forming a supporting sealing resin material which fills said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said parts of said external electrodes for supporting said external electrodes.

73. The method as claimed in claim 60, further comprising the step of :

completely removing said high rigidity plate from said

interconnection board, after said interconnection board is fabricated on said high rigidity plate ;

forming a supporting plate having plural holes, into which said external electrodes are inserted, so that said supporting plate extends in parallel to said second surface of said buffer layer to form an inter-space between said supporting plate and said second surface of said buffer layer ; and

forming a supporting sealing resin material which fills said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said parts of said external electrodes for supporting said external electrodes.

74. The method as claimed in claim 60, further comprising the step of :

completely removing said high rigidity plate from said interconnection board, after said interconnection board is fabricated on said high rigidity plate ;

bonding plural generally column shaped electrically conductive layers to said interconnection board via an adhesive ; and

forming external electrodes on said plural generally column shaped electrically conductive layers so that said external electrodes are electrically connected through said plural generally column shaped electrically conductive layers to said interconnection board.

75. The method as claimed in claim 74, further comprising the step of :

forming a supporting plate having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board ; and

forming a supporting sealing resin material which fills said inter-space and surrounds both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

76. The method as claimed in claim 60, further comprising the step of :

mounting at least a semiconductor chip on said interconnection board ; and

completely removing said high rigidity plate from said interconnection board.

77. The method as claimed in claim 60, further comprising the step of :

mounting at least a semiconductor chip on said interconnection board ;

forming at least a heat spreader on said at least semiconductor chip ; and

completely removing said high rigidity plate from said interconnection board.

78. The method as claimed in claim 60, further comprising the step of :

mounting at least a semiconductor chip on said interconnection board ; and

selectively removing said high rigidity plate from said interconnection board to form plural generally column shaped electrically conductive layers on said interconnection board.

79. The method as claimed in claim 60, further comprising the step of :

mounting at least a semiconductor chip on said interconnection board ;

forming at least a heat spreader on said at least semiconductor chip ; and

selectively removing said high rigidity plate from said interconnection board to form plural generally column shaped electrically conductive layers on said interconnection board.

Add B7